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LIMBACH & LIMBACH L.L.P.
2001 Ferry Building, San Francisco, CA 94111
415/433-4150

Address to:
Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

Attorney's Docket No. NSC1-H1200
[P04776]
First Named Inventor VLADISLAV VASHCHENKO

UTILITY PATENT APPLICATION TRANSMITTAL
(under 37 CFR 1.53(b))

SIR:

Transmitted herewith for filing is the patent application entitled:
DIAC ESD PROTECTION STRUCTURE FOR CMOS TECHNOLOGY

CERTIFICATION UNDER 37 CFR § 1.10

I hereby certify that this New Application and the documents referred to as enclosed herein are being deposited with the United States Postal Service on this date September 11, 2000 , in an envelope bearing "Express Mail Post Office To Addressee" Mailing Label Number EL387336848US addressed to: Box Patent Application, Assistant Commissioner for Patents, Washington, D.C. 20231.

SUSAN OZANNE — Susan Ozanne
(Name of person mailing paper) (Signature)

Enclosed are:

I. X Transmittal Form (two copies required)

II. The papers required for filing date under CFR § 1.53(b):
i. 12 Pages of specification (including claims and abstract);
ii. 1 Sheets of drawings.
__ formal X informal

III. Declaration or oath

a. X Newly executed (original or copy)

IV. __ Microfiche Computer Program (Appendix, see 37 CFR 1.96)

V. __ Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
i. __ Computer Readable Copy
ii. __ Paper Copy (identical to computer copy)
iii. __ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

VI. X An assignment of the invention to National Semiconductor Corporation is attached (including Form PTO-1595).

i. __ 37 CFR 3.73(b) Statement (when there is an assignee)

VII. __ Power of Attorney

VIII. __ An Information Disclosure Statement (IDS) is enclosed, including a PTO-1449 and copies of __ references.

IX. __ Preliminary Amendment.

X. _X_ Return Receipt Postcard (MPEP 503 -- should be specifically itemized)

XI. __ Other

XII. FOREIGN PRIORITY
[] Priority of application no. _ filed on _ in _ is claimed under 35 USC 119.

The certified copy of the priority application:
- is filed herewith; or
- has been filed in prior application no. _ filed on _, or
- will be provided.

__ English Translation Document (if applicable)

XIII. **FEE CALCULATION**

a. __ Amendment changing number of claims or deleting multiple dependencies is enclosed.

CLAIMS AS FILED

	Number Filed	Number Extra	Rate	Basic Fee ($690)
Total Claims	7 - 20	* 0	x $18.00	0
Independent Claims	1 - 3	* 0	x $78.00	0
__ Multiple dependent claim(s), if any			$260.00	0

*If less than zero, enter "0".

Filing Fee Calculation $690

50% Filing Fee Reduction (if applicable) $0

XIV. Small Entity Status
a. __ A small entity statement is enclosed.
b. __ A small entity statement was filed in the prior nonprovisional application and such status is still proper and desired.
c. __ is no longer claimed.

XV. Other Fees
_X_ Recording Assignment [$40.00] $40
__ Other fees
Specify _____ $0

Total Fees Enclosed $730

XVI. Payment of Fees
_X_ Check(s) in the amount of $ 730 enclosed.
__ Charge Account No. 12-1420 in the amount of $__.
A duplicate of this transmittal is attached.

XVII. All correspondence regarding this application should be forwarded to the undersigned attorney:

Mayumi Maeda
Limbach & Limbach L.L.P.
2001 Ferry Building
San Francisco, CA 94111
Telephone: 415/433-4150
Facsimile: 415/433-8716

XVIII. Authorization to Charge Additional Fees

X The Commissioner is hereby authorized to charge any additional fees (or credit any overpayment) associated with this communication and which may be required under 37 CFR § 1.16 or § 1.17 to Account No. 12-1420. **A duplicate of this transmittal is attached.**

LIMBACH & LIMBACH L.L.P.

September 11, 2000
(Date)

By: _____
Mayumi Maeda
Registration No. 40,075
Attorney(s) or Agent(s) of Record

Attorney Docket No. NSC1-H1200
[P04776]

PATENT

ELECTROSTATIC DISCHARGE (ESD) PROTECTION STRUCTURE

INVENTORS: Vladislav Vashchenko, Peter J. Hopper and Manuel Carneiro

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to semiconductor device structures and, in particular, to electrostatic discharge protection structures for use with integrated circuits.

2. Description of the Related Art

Electrostatic discharge (ESD) protection devices are commonly employed in an integrated circuit (IC) to protect electronic devices in the IC from spurious pulses of excessive voltage (e.g., an ESD event, Human Body Model [HBM] event, or Electrical Overstress [EOS] event). See, for example, S.M. Sze, *Electrostatic Discharge Damage,* in VLSI Technology, Second Edition, 648-650 (McGraw Hill, 1988). A variety of conventional ESD protection devices that make extensive use of diodes, metal-oxide-semiconductor field effect transistors (MOSFETs), and bipolar transistors are known in the field. For example, conventional ESD protection devices for use with CMOS integrated circuits include Grounded Gate MOS (GGMOS) ESD protection structures and Low Voltage Silicon Controlled Rectifier (LVSCR) ESD protection structures. Descriptions of these and other conventional ESD protection structures are available in Haigang, et al., *A Comparison Study of ESD Protection for RFICs: Performance vs. Parasitics*, 2000 IEEE Radio Frequency Integrated Circuits Symposium, 235-237 (2000); U.S. patent application for "MOSFET Structure For Use in ESD Protection Devices" (filed July 17, 2000; application number not yet assigned) and U.S. Patent Application No. 09/205,110 (filed December 3, 1998), each of which is hereby fully incorporated by reference.

Conventional MOSFET structures are designed to exhibit breakdown characteristics only at voltages well above their standard operating supply voltage. However, during an ESD event, GGMOS ESD structures exhibit current conduction via a parasitic lateral bipolar mechanism. For a further description of current conduction in GGMOS ESD structures via a parasitic lateral bipolar mechanism, see E. A. Amerasekera et al., *ESD in Silicon Integrated Circuits*, sections 3.5.2 and 3.6 (John Wiley & Sons, 1995), which are hereby fully incorporated by reference.

ESD events can be of either a negative polarity or a positive polarity. Conventional GGMOS or LVSCR ESD protection structures can only protect electronic devices in an IC from a single polarity ESD event. Thus, two such structures are required to protect electronic devices in an IC from ESD events of both polarities.

The ESD protection capability of ESD protection devices is characterized by their snapback holding voltage and their maximum snapback current. ESD protection capability is improved at lower snapback holding voltages and higher maximum snapback current. Conventional GGMOS and LVSCR ESD protection structures operate via an avalanche-injection conductivity modulation mechanism. This mechanism, however, provides a relatively high snapback holding voltage and a relatively low snapback current.

Still needed in the field, therefore, is an ESD protection structure that can protect electronic devices in an IC from ESD events of both positive and negative polarities, has a low snapback holding voltage and a high maximum snapback current.

SUMMARY OF THE INVENTION

The present invention provides an ESD protection structure for use with ICs that can protect electronic devices in an IC from ESD events of both positive and negative polarities, has a low snapback holding voltage and a high maximum snapback current.

ESD protection structures for use with ICs according to the present invention include a semiconductor substrate (e.g., a silicon substrate) of a first conductivity type (typically P-type), a first well region of a second conductivity type (typically N-type) disposed in the semiconductor substrate, and a second well region, also of the second conductivity type, disposed in the semiconductor substrate. The first and second well regions are separated by a gap region of the first conductivity type that is disposed in the semiconductor substrate.

Also included in ESD structures according to the present invention are a first floating region and a second floating region, each of the second conductivity type, disposed in the first well region and second well region respectively. The first and second floating regions are adjacent to the gap region. The ESD structures further include first and second contact regions of the first conductivity type disposed on the first and second well regions, respectively, and spaced apart from the first and second floating regions, respectively. In addition, the ESD structures include first and second contact regions of the second conductivity type that are also disposed on the first and second well regions, respectively, and also spaced apart from the first and second floating regions, respectively.

ESD protection structures according to the present invention can be thought of as a variant of a DIAC structure that provides ESD protection capability by the distinctive addition of first and second floating regions, and a P-type contact region and an N-type contact region in each of the first and second well regions.

During operation, ESD protection structures according to the present invention undergo primary breakdown via a low current avalanche breakdown mechanism in the gap region between the first and second floating regions. Following this low current avalanche breakdown, and when the current has exceeded a critical switching value, the ESD protection structures exhibit "double injection" of holes and electrons from an N-type and a P-type contact region, one in each of the first and second well regions, to attain a high maximum snapback current. This high maximum snapback current is attributed

to mutual space charge neutralization and conductivity modulation in the gap region (and an associated reduction in the electric field).

An advantage of ESD protection structures according to the present invention is that they are symmetrical (i.e., each of the first and second well regions has both an N-type contact region and a P-type contact region disposed therein). The ESD protection structures can, therefore, protect electronic devices in an IC from ESD events of both a negative and a positive polarity. ESD protection structures according to the present invention can be manufactured using conventional semiconductor manufacturing process techniques (e.g., 0.18 micron CMOS process technologies) and are, therefore, compatible for use with CMOS integrated circuits.

BRIEF DESCRIPTION OF THE DRAWINGS

A better understanding of the features and advantages of the present invention will be obtained by reference to the following detailed description that sets forth illustrative embodiments, in which the principles of the invention are utilized, and the accompanying drawings, of which:

FIG. 1 is a combined cross-sectional and electrical schematic depiction of an ESD protection structure in accordance with the present invention.

FIG. 2 is a current versus voltage (I-V) graph illustrating the simulated electrical behavior of an ESD protection structure according to the present invention formed using a 0.18 micron CMOS process technology (curve A) and a conventional GGMOS ESD protection structure formed using the same 0.18 micron CMOS process technology (curve B).

DETAILED DESCRIPTION OF THE INVENTION

To be consistent throughout the present specification and for clear understanding of the present invention, the following definitions are provided for terms used therein:

The terms "dopant" and "dopants" refer to donor and acceptor impurity atoms (e.g., boron [B], phosphorous [P], arsenic [As] and indium [In]), which are intentionally introduced into a semiconductor substrate (e.g., a silicon wafer) in order to change the substrate's charge-carrier concentration. See, R.S. Muller and T.I. Kamins, *Device Electronics for Integrated Circuits 2nd Edition,* 11-14 (John Wiley and Sons, 1986) for a further description of dopants.

FIG. 1 illustrates an ESD protection structure 100 for use with ICs according to the present invention. ESD protection structure 100 includes a P-type semiconductor substrate 102 (e.g., a P-type silicon substrate, a P-type epitaxial silicon substrate or a high resistance P-type silicon substrate). The dopant concentration in the semiconductor substrate 102 can be any conventional concentration known in the art. ESD protection structure 100 also includes a first N-type well region 104 and a second N-type well region 106 disposed in the semiconductor substrate 102. The dopant concentrations of the first and second N-type well regions are essentially identical. The dopant concentrations and dimensions of the first and second N-type well regions depend on the semiconductor manufacturing process technology employed to create the ESD protection structure. A typical dopant concentration for ESD protection structures created with an 0.18 micron CMOS process technology is, however, in the range of 1E17 atoms/cm^2 to 1E20 atoms/ cm^2, while a typical depth of the first and second N-type well regions is 1.25 microns.

The first N-type well region 104 and second N-type well region 106 are separated by a P-type gap region 108 disposed in the semiconductor substrate 102. For a 0.18 micron CMOS process technology, the P-type gap region 108 separates the first N-type well region 104 from the second N-type well region 106 by a minimum distance in the range of 0.18 microns to 0.25 microns. The P-type gap region 108 functions as a discharge space during an ESD event.

Also included in ESD protection structure 100 are a first N-type floating region 110 disposed in the first N-type well region 104 adjacent to the P-type gap region 108 and a second N-type floating region 112 disposed in the second N-type well region 106 adjacent to the P-type gap region 108. The dopant concentrations of the first and second N-type floating regions 110, 112 are

greater than that of the first and second N-type well regions 104, 106. The first and second N-type floating regions 110, 112, therefore, provide a sharp P/N junction between themselves and the P-type gap region 108. This sharp P/N junction provides an ESD protection structure 100 with a low trigger voltage (e.g., a trigger voltage in the range of 6 volts to 8 volts). In the absence of first and second N-type floating regions 110, 112, the trigger voltage would be unacceptably high (e.g., in the range of 15 volts to 25 volts) due to the presence of only the relatively smooth P/N junctions that are formed between the N-type well regions and the P-type gap region during conventional CMOS technology processing.

ESD protection structure 100 also includes four contact regions: (i) a first P-type contact region 114 disposed on the first N-type well region 104 that is spaced apart from the first N-type floating region 110; (ii) second P-type contact region 116 disposed on the second N-type well region 106 and spaced apart from the second N-type floating region 112; (iii) a first N-type contact region 118 disposed on the first N-type well region 104 and spaced apart from the first N-type floating region 110; and (iv) a second N-type contact region 120 disposed on the second N-type well region 106 and spaced apart from the second N-type floating region 112. The ESD protection structure 100 of FIG. 1 further includes a first electrical contact 122 connected to the first P-type contact region 114, the first N-type contact region 118, and an IC. For example, first electrical contact 122 can be connected to a line, pin or bus of an IC, for which ESD protection is desired. In addition, ESD protection structure 100 includes a second electrical contact 124 connected to the second P-type contact region 116, the second N-type contact region 120 and to ground (GND). First and second electrical contacts 122, 124 can be formed using conventional semiconductor manufacturing process techniques, including metal silicidation or metal deposition.

During an ESD event, an ESD pulse arriving at the first electrical contact 122 will provide a low level of current flow across the P-type gap region 108. This low level of current flow initiates primary breakdown of the ESD protection structure 100 via low current avalanche breakdown of the P-type gap

region 108 between the first N-type floating region 110 and the second N-type floating region 112. This avalanche breakdown occurs at a trigger voltage that is dependent on the dopant profiles of the first and second N-type floating regions 110, 112 and the P-type gap region 108, as well as the separation distance between the first N-type well region 104 and the second N-type well region 106.

The structural arrangement of the first and second N-type floating regions 110, 112 and the P-type gap region 108 creates an NPN sub-structure in the center of the ESD protection structure 100. Since the distance separating the first and second N-type floating regions 110, 112 (i.e., the width of the P-type gap region 108) is relatively short, the space charge region available in the P-type gap region 108 is limited by the presence of the first and second N-type well regions 104, 106. The breakdown voltage of the P-type gap region 108 is, therefore, to an extent proportional to the separation between the first and second N-type well regions 104, 106 (i.e., to the width of the P-type gap region 108). Therefore, the triggering voltage of the ESD protection structure can be tuned to suit particular needs by providing a gap region of the appropriate width.

As the ESD event continues, the current increases to a critical switching level whereupon the ESD protection structure enters a switching state. In the switching state, "double injection" occurs from a single contact region in both of the N-type well regions. By providing both a P-type contact region and an N-type contact region in each N-type well region (i.e., by providing "double junctions"), ESD protection structures according to the present invention are capable of operating via a "double injection" mechanism. This "double injection" mechanism involves the injection of both holes and electrons, one from each side of the ESD protection structure, regardless of the polarity of an ESD pulse. In other words, depending on the polarity of ESD event, either holes are injected from the first P-type contact region or electrons are injected from the first N-type contact region. At the same time, however, either electrons are injected from the second N-type contact region or holes are injected from the second P-type contact region. This double injection (i.e., the

injection of holes from a contact region in one of the well regions, while the injection of electrons occurs from a contact region in the other well region) results in mutual space charge neutralization (i.e., the positive and negative currents of the holes and electrons compensate one another). This mutual space charge neutralization results in a conductivity modulation in the gap region (and an associated reduction in the electric field) that supports the attainment of relatively high maximum snapback currents.

ESD protection structures for use with ICs according to the present invention can, if desired, be formed with the first and second N-type well regions in an elongated "finger" arrangement (with a finger length of, for example 50 microns to 100 microns) or as multiple connected fingers.

FIG. 2 illustrates the I-V characteristics obtained from a numerical simulation for an ESD protection structure according to the present invention formed using a 0.18 micron CMOS process technology (curve A), and a conventional GGMOS ESD protection structure formed using the same 0.18 micron CMOS process technology (curve B). The current represented in FIG. 2 is, for the case of the conventional GGMOS, drain current and, for the case of ESD protection structures according to the present invention, the current through the second well region. The voltage represented in FIG. 2 is, for the case of the conventional GGMOS, the drain-to-source voltage and, for the case of ESD protection structures according to the present invention, the voltage between the first and second well regions.

For the conventional GGMOS ESD protection structure of FIG. 2, the snap-back holding voltage is approximately 6 volts. For the ESD protection structure according to the present invention, however, the snap-back holding voltage is less than 2 volts. In addition, the maximum snapback current for the ESD protection structure according to the present invention is 8 to 10 times greater than that of the conventional GGMOS ESD protection structure. The lower snapback holding voltage and higher maximum snapback current of ESD protection structures according to the present invention, therefore, provide an increase in ESD protection capability of approximately 10 times. This 10-fold increase in ESD protection capability allows the use of ESD protection

structures of 10 times less area to obtain the same level of ESD protection (e.g., protection against a 2-4KeV pulse) as a conventional GGMOS ESD protection structure or the provision of increased ESD protection for an ESD protection device of the same area.

It should be understood that various alternatives to the embodiments of the invention described herein may be employed in practicing the invention. It is intended that the following claims define the scope of the invention and that structures within the scope of these claims and their equivalents be covered thereby.

WHAT IS CLAIMED IS:

1. An ESD protection structure for use with an integrated circuit comprising:

a semiconductor substrate of a first conductivity type;

a first well region of a second conductivity type disposed in the semiconductor substrate;

a second well region of the second conductivity type disposed in the semiconductor

a gap region of the first conductivity type disposed in the semiconductor substrate and separating the first well region from the second well region,

a first floating region of the second conductivity type disposed in the first well region adjacent to the gap region;

a second floating region of the second conductivity type disposed in the second well region adjacent to the gap region;

a first contact region of the first conductivity type disposed on the first well region and spaced apart from the first floating region;

a second contact region of the first conductivity type disposed on the second well region and spaced apart from the second floating region;

a first contact region of the second conductivity type disposed on the first well region and spaced apart from the first floating region;

a second contact region of the second conductivity type disposed on the second well region and spaced apart from the second floating region.

2. The ESD protection structure of claim 1 further comprising:

a first electrical contact connected to the first contact region of the first conductivity type, the first contact region of the second conductivity type, and the integrated circuit; and

a second electrical contact connected to the second contact region of the first conductivity type, the second contact region of the second conductivity type and to ground.

3. The ESD protection structure of claim 1, wherein the first conductivity type is P-type and the second conductivity type is N-type.

4. The ESD protection structure of claim 1, wherein the dopant concentrations of the first floating region and the second floating region are greater than the dopant concentrations of the first well region and the second well region.

5. The ESD protection structure of claim 4, wherein the dopant concentration of the first well region and the second well region is at least 1E17 atoms per cm^2.

6. The ESD protection structure of claim 1, wherein the gap region separates the first well region from the second well region with a minimum distance in the range of 0.18 microns to 0.25 microns.

7. The ESD protection structure of claim 1, wherein the first well region and the second well region are disposed in the semiconductor substrate in an elongated finger configuration.

ABSTRACT OF THE DISCLOSURE

An ESD protection structure for use with ICs that can protect from ESD events of both positive and negative polarities, has a low snapback holding voltage and a high maximum snapback current. The ESD protection structure includes a semiconductor substrate of a first conductivity type (typically P-type), and first and second well regions of a second conductivity type (typically N-type) disposed in the substrate. The first and second well regions are separated by a gap region of the first conductivity type in the substrate. Also included are first and second floating regions (of the second conductivity type) disposed in the first and second well regions adjacent to the gap region, respectively. The ESD protection structure also includes first and second contact regions of the first conductivity type disposed on the first and second well regions, respectively, and spaced apart from the first and second floating regions, respectively. The ESD protection structure further includes first and second contact regions of the second conductivity type disposed on the first and second well regions, respectively, and spaced apart from the first and second floating regions, respectively. During operation, the ESD protection structure undergoes primary breakdown by low current avalanche breakdown of the gap region between the first and second floating regions, followed by "double injection" of both holes and electrons, thereby providing for a low snapback holding voltage and a high maximum snapback current. The symmetrical nature of the ESD protection structure provides for protection from both positive and negative ESD events.

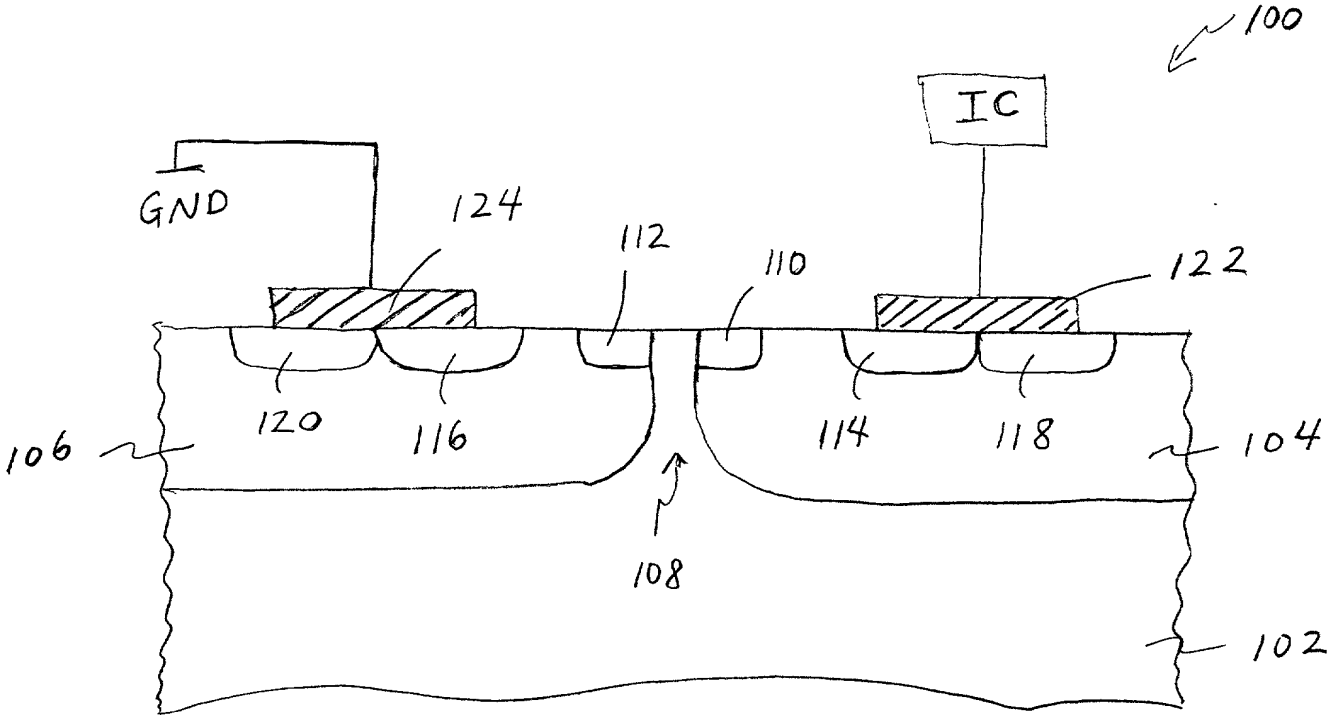
100
IC
GND
124
112
110
122
120
116
114
118
106
104
108
102

FIG. 1

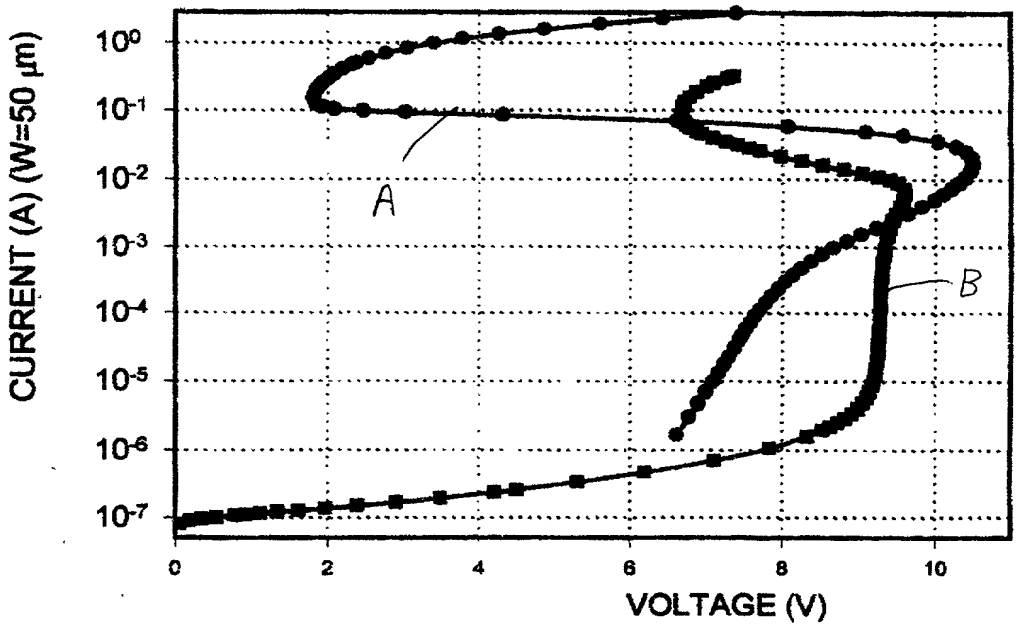
CURRENT (A) (W=50 μm)
10⁰
10⁻¹
10⁻²
10⁻³
10⁻⁴
10⁻⁵
10⁻⁶
10⁻⁷
0
2
4
6
8
10
VOLTAGE (V)
A
B

FIG. 2

Declaration for Patent Application English Language Declaration		
	Attorney Docket No.	NSC1-H1200-(US)
	First Name Inventor	Vladislav Vashchenko
	COMPLETE IF KNOWN:	
[X] Submitted with initial filing [ ] Submitted after initial filing (surcharge required 37 CFR 1.16(e))	Application No.	
	Filing Date	
	Group Art Unit	N/A
	Examiner	Not Yet Assigned

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

ELECTROSTATIC DISCHARGE (ESD) PROTECTION STRUCTURE

the specification of which (check one)

[X] is attached hereto.

[ ] was filed on _____
as United States Application No. or PCT International Application No. _____
and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information which is material to patentability as defined in 37 CFR 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. 119 (a)-(d) or 365(b) of any foreign applications(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate or any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

			Priority Not Claimed	Certified Copy Attached	
				YES	NO
_____ (Number)	_____ (Country)	_____ (Filing Date)	[ ]	[ ]	[ ]
_____ (Number)	_____ (Country)	_____ (Filing Date)	[ ]	[ ]	[ ]
_____ (Number)	_____ (Country)	_____ (Filing Date)	[ ]	[ ]	[ ]

[ ] Additional prior foreign applications are listed on a supplemental data sheet attached hereto.

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)

☐ Additional U.S. provisional applications are listed on a supplemental data sheet attached hereto.

I hereby claim the benefit under 35 U.S.C. 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) Patent No. (if applicable):
(Application Serial No.)	(Filing Date)	(Status) Patent No. (if applicable):
(Application Serial No.)	(Filing Date)	(Status) Patent No. (if applicable):

☐ Additional U.S. or PCT international application numbers are listed on a supplemental data sheet attached hereto.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor	
Vladislav Vashchenko	
Sole or first inventor's signature [signature]	Date 9. 7. 00
Residence 39939 Stevenson Cmn., Fremont, California 94538	
Citizenship Russia	
Post Office Address 39939 Stevenson Cmn. Fremont, California 94538	

Full name of second inventor	
Peter J. Hopper	
Second inventor's signature [signature]	Date 9.7.00
Residence 4327 Verdigris Circle, San Jose, California 95134	
Citizenship United Kingdom	
Post Office Address 4327 Verdigris Circle San Jose, California 95134	

Full name of third inventor Manuel Carneiro	
Third inventor's signature	Date 9/7/00
Residence 1117 Casual Way, San Jose, California 95120	
Citizenship United States of America	
Post Office Address 1117 Casual Way San Jose, California 95120	

Full name of fourth inventor, if any	
Fourth inventor's signature	Date
Residence	
Citizenship	
Post Office Address	

Full name of fifth inventor, if any	
Fifth inventor's signature	Date
Residence	
Citizenship	
Post Office Address	

Full name of sixth inventor, if any	
Sixth inventor's signature	Date
Residence	
Citizenship	
Post Office Address	